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328654(28)

B. E. (Sixth Semester) Examination April-May 2021

(New Scheme)

(Et&T Branch)

VLSI DESIGN

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all questions. Part (a) of each question is compulsory, which is of 2 marks. Attempt any* **two** *parts from (b), (c) and (d) each is of 7 marks. Assume suitable data wherever necessary. Draw the diagram to support your answer if required.*

Unit-I

1. (a) What is Moore's law? 2

(b) Consider an n-channel MOS system that is characterized by x_{ox} = 100 Å and Na = $10^{15}/cm^3$. An n-type poly gate is used with $N_{d, poly} = 10^{19}/cm^3$. The fixed oxide charge is approximated as $Q_f = q\,(10^{11})$ c/cm^2 and is the dominant oxide charge term, and the acceptor ion implant dose is assumed to be $D_I \approx 2\times10^{12}$ /cm^2. Determine the threshold voltage. 7

(c) Explain the term switching intervals and derive an expression for fall time (t_f) in CMOS inverters. 7

(d) Draw the complete VLSI Design flow for programmable logic devices and Application Specific Integrated Circuits (ASIC). 7

Unit-II

2. (a) Write the significance of Euler graph to draw stick diagram or layout for any complex logic circuit. 2

(b) Describe photolithography process for VLSI circuits and role of positive & negative photoresist to draw various patterns. 7

(c) Explain the basic sequence of processes to fabricate *n*-well CMOS inverter. 7

(d) Write the MOSIS Lamda (λ) based layout design rules for active area, polysilicon, metal and contacts. 7

Unit-III

3. (a) Write the difference between stick diagram & layout representation of the circuit. 2

(b) Draw the pass transistor based circuit diagram & layout for 4 : 1 multiplexer. 7

(c) Draw the circuit diagram for 6 T SRAM & explain the read and write operations. 7

(d) Draw the CMOS layout of J-K flip-flop. 7

Unit-IV

4. (a) Write the critical difference between Concurrent & Sequential Assignment Statements. 2

(b) Consider the function $f(x_1, x_2, x_3) = \sum m$

$(2, 3, 4, 6, 7)$. Show how it can be realized using 2, two input LUT's only. 7

(c) With the use of Generate syntax, write the VHDL code to design 16 : 1 multiplexer using 4 : 1 multiplexer as a component. 7

(d) Explain process statements of VHDL, including general syntax of process, sensitivity list, process declarative items, sequential statements and example. 7

Unit-V

5. (a) Define the term test vectors in test bench source code. 2

(b) Write a VHDL code of Moore type FSM (Finite State Machine) for serial adder. 7

(c) Write a VHDL code to design Mealy FSM (Finite State Machine) to detect a bit sequence 101. 7

(d) Write a VHDL code which describes a simple test bench for half adder. 7